response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

3. (Canceled)

4. (Previously amended) The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. (Previously amended) The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

6. (Canceled)

7. (Canceled)

8. (Cancel) A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

9. (Canceled)

PAGE 3/8 * RCVD AT 7/30/2004 4:10:28 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:408 4749082 * DURATION (mm-ss):01-36

10. (Previously amended) A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. (Currently amended) An integrated circuit comprising:

means for receiving from an external tester test vectors for ~~the~~ testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. (Currently amended) A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. (Currently amended) The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further comprising ~~the test response analysis unit~~:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

PAGE 4/8 * RCVD AT 7/30/2004 4:10:28 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:408 4749082 * DURATION (mm-ss):01-36

outputting said compact representation to the external tester.

PAGE 5/8 * RCVD AT 7/30/2004 4:10:28 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:408 4749082 * DURATION (mm-ss):01-36